IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re:		
	Application of:	Subramanian et al.
	Serial No.:	10/534,903
	Filed:	May 16, 2005
	For:	Mailbox Interface Between Processors
	Group Art Unit:	2154
	Examiner:	Jeong S. Park
	Our Docket No.:	1890-0248

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated on the attached sheets. This paper is filed by the Attorney of Record.

I. Reasons for Review

A first clear error in the Examiner's rejection of claim 9 is that the Examiner has not provided a clearly articulated reason for modifying U.S. Patent No. 5,210,828 to Bolan et al. (hereinafter "Bolan") in view of U.S. Patent No. 6,151,644 to Wu (hereinafter "Wu"), with the teachings of European Patent Document EP 0599257 to Juri (hereinafter "Juri"). In other words, even if one modified the teachings of Bolan with the teachings of Wu as proposed by the Examiner, the Examiner has not provided any clearly articulated reason to further modify Bolan/Wu with the teachings of Juri.

A second clear error in the Examiner's rejection is that the Examiner has not identified where any of Bolan, Wu or Juri teach or suggest a control unit arranged to "store at least a

first data packet of the first message in the ancillary memory without storing the first data packet in the main memory and store at least one other data packet of the first message in the main memory".

A. No Reason to Combine

The claimed invention involves an apparatus that is configured to, among other things "store at least a first data packet of [a] first message in [an] ancillary memory without storing the first data packet in the main memory". As claimed, the main memory is of the first type, and the second memory is of a different type.

The Examiner has admitted that Bolan does not teach storing a data packet in an ancillary memory "*without storing the ... data packet in the main memory*". (Final Office Action at p.12). To satisfy this element, the Examiner cites the teachings of Wu. In particular, the Examiner asserts that Wu teaches storing data in a number of registers PB0-PBN, wherein the packet buffer PB0 can be considered the "ancillary memory" as claimed, and the packet buffers PB1-PBN can be considered the "main memory" as claimed. (See Final Office Action at p.13; see also Wu at Fig. 2). The Examiner then asserts that portions of a packet (message?) are stored in the ancillary memory (PB0) and the main memory (PB1-PBN).

The Examiner correctly noted, however, that *even* if Bolan were modified to use the structure PB0-PBN of Wu as the main and ancillary memories, the resulting combination would still fail to include the feature "wherein the main memory is of a first type, and the second memory is of a second type that is *different* than the first type". (See Final Office Action at p.5). To address this deficiency of Bolan/Wu, the Examiner has cited the teachings

of Juri. Juri teaches using an ancillary memory in a video signal recording device that employs bit reduction. (Final Office Action at pp.5-6 & 13-14).

The Examiner provided the following articulation of a reason to combine the teachings of Bolan/Wu with the teachings of Juri:

> It would have been obvious for one of ordinary skill in the art at the time the invention to modify Bolan in view of Wu to include an overflow memory as taught by Juri in order to efficiently process the data overflown from the main memory.

(Final Office Action at p.5). As best understood, the Examiner appears to allege that one would replace the packet buffer PB0 of Wu (i.e. the ancillary memory) with the overflow memory of Juri (which appears to be a FIFO type of memory). Although not articulated, such a replacement would result in two types of memories because the main memory would remain the packet buffers PB1-PBN of Wu. However, the Examiner has not identified any motivation, suggestion, advantage, reason, or other purpose to replace one of the packet buffers of Wu with the ancillary memory of Juri.

1. *No Advantage Tied to Using Specific Type of Memory*

The only reason provided by the Examiner for making the modification of Bolan/Wu with Juri is to "efficiently process the data overflown from the main memory". (Final Office Action at p.6). However, this allegation does not identify or support any relationship between efficiently processing of overflow data with a memory of a *certain type*. In other words, while Juri teaches an ancillary memory, it does not teach that the ancillary memory should be of a certain *type* in order to "efficiently process the data overflown from the main memory". Because Juri fails to teach that a certain type of overflow memory is efficient, there is no rational reason to believe, from the teachings of Juri or otherwise, that using a certain type of

overflow memory is more efficient than other types of overflow memory. The Examiner has not provided *any* support for the allegation that replacing the buffer PB0 of Wu with the ancillary memory of Juri will result in increased efficiency.

2. *Juri Relates to Specific Issues Not Relevant to Bolan/Wu*

Bolan and Wu are directed to completely different fields than that of Juri. Bolan is directed to communications between co-processors, and a mailbox facility for such communications. (Bolan at col. 1, lines 48-50). Wu is directed to a buffer management system for a network packet buffer. (Wu at col. 2, lines 59-62). While the technical fields of Bolan and Wu are marginally related, neither field relates to the technology discussed in Juri.

In particular, unlike Bolan and Wu, Juri is directed to a video signal recording apparatus and method. (See Juri at Fig. 1a, and at col. 1, lines 5-8). The video signal recording apparatus of Juri uses bit rate reduction suitable for devices such as VCRs. (Col. 1, lines 44-49). To this end, Juri teaches the storage of video frames on a tape. (See Fig. 1a). The data manipulation of Juri is completely unrelated to interprocessor communication (i.e. Bolan), or even network packet buffers (i.e. Wu). No one of ordinary skill in the interprocessor communication art or network buffer art would have reason to refer to Juri for any relevant teaching regarding the use of an ancillary memory, and certainly not for a *type* of ancillary memory.

B. *No Teaching of Splitting a Message Between Memories*

The Examiner has not identified where any of Bolan, Wu or Juri teach or suggest a control unit arranged to "store at least a first data packet of the first message in the ancillary

memory ... and store at least one other data packet of the first message in the main memory". To address this limitation, the Examiner relies on the teaching of Wu, as discussed further above. In particular, the Examiner identifies the memories PB1 to PBN as the "main memory", and PB0 of Wu as being the ancillary memory. The Examiner then alleges:

> When receive module receives a large packet, which is larger than can be stored in a single packet buffer, it reserves the next unoccupied packet buffer, wherein the packet buffer PB0 is interpreted as [the] ancillary memory and the packet buffer PB1 as the main memory (see, e.g., col. 4, lines 30-63).
>
> Therefore the first portion of the large packet is stored at ... PBO ... and the rest of the large packet are stored at ... PB1-PBN....

However, contrary to the Examiner's assertion, col. 4 of Wu does *not* teach splitting a large packet (or message) across multiple packet buffers. Wu merely teaches placing a large packet (i.e. the *entire* large packet) in the next buffer. (Wu at col. 4, lines 30-63). Wu does not teach splitting portions of a packet, or portions of single message, across different buffers. Because the Examiner has based the rejection of claim 9 on the misinterpretation that Wu teaches storing different portions of the same packet/message in two different buffers, there is clear error in the rejection of claim 9.

C. *Conclusion*

For all of the reasons discussed above, it is respectfully submitted that the obviousness rejection of claim 9 should be withdrawn. All of the other claims in the application include limitations substantially identical to those discussed above, and are therefore similarly in a condition for allowance.

Respectfully Submitted,

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